CMOS DECADE 7-SEGMENT DECODERS

FEATURES

- Decade Counter and 7-Segment Decoder in One Package
- Easily Interfaced with 7-Segment Display Types
- Direct Reset
- Display Enable Function (4026AB)
- Ripple Blanking and Lamp Test Functions (4033AB)
- Trigger from either Edge of Clock Input
- Carry Output for Cascading Stages
- Fully Static Operation - DC to 5MHz @ 10Vdc

DESCRIPTION

These two devices each consist of a 5-stage Johnson Decade Counter and an Output Decoder which converts the Johnson code to a 7-segment decoded output for driving each stage in a numerical display. A high Reset signal clears the decade counter to its zero count. The counters have interchangeable Clock and Clock Enable lines for incrementing on either a positive-going or negative-going transition, respectively. Antilock gating is provided on the Johnson counter, thus assuring proper counting sequence. The Carry-Out (C_{OUT}) signal completes one cycle every ten clock input cycles and is used to directly clock the succeeding decade in a multi-decade counting chain.

4026AB

When the Display Enable is low, the seven decoded outputs are forced off regardless of the state of the counter. Activation of the display only when required results in significant power savings. This system also facilitates implementation of display-character multiplexing.

The Carry Out and ungated "C-segment" signals are not gated by the Display Enable and therefore are available continuously. This feature is a requirement in implementation of certain divider functions such as divide-by-60 and divide-by-12.

4033AB

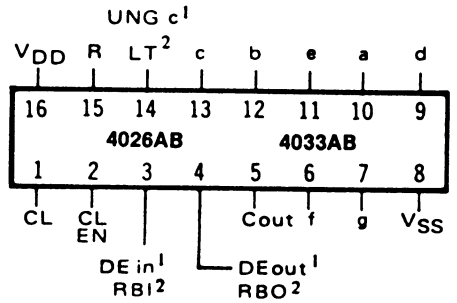
The 4033AB has provisions for automatic blanking of the non-significant zeros in a multi-digit decimal number which results in an easily readable display consistent with normal writing practice. For example, the number 0050.0700 in an eight digit display would be displayed as 50.07. Zero suppression on the integer side is obtained by connecting the RBI terminal of the 4033AB associated with the most significant digit in the display to a "low-level" voltage and connecting the RBO terminal of that stage to the RBI terminal of the 4033AB in the next-lower-significant position in the display. This procedure is continued for each succeeding 4033AB on the integer side of the display. On the fraction side of the display the RBI of the 4033AB associated with the least significant digit is connected to a "low-level" voltage and the RBO of the 4033AB is connected to the RBI terminal of the 4033AB in the next-more-significant-digit position. Again, this procedure is continued for each 4033AB on the fraction side of the display.

In a purely fractional number the zero immediately preceding the decimal point can be displayed by connecting the RBI of that stage to a high voltage (instead of to the RBO of the next-more-significant stage). For Example: optional zero - 0.7346.

Likewise, the zero in a number such as 763.0 can be displayed by connecting the RBI of the 4033AB associated with it to a "high-level" voltage.

A "high" Lamp Test signal turns on all outputs.

CONNECTION DIAGRAM
(all packages)



[1] 4026AB
[2] 4033AB

Add suffix for package:

C 16-pin Cerdip

RECOMMENDED OPERATING CONDITIONS

For maximum reliability:

DC Supply Voltage	$V_{DD} - V_{SS}$	3 to 15	Vdc
Operating Temperature C	T_A	-55 to +125	°C

ELECTRICAL CHARACTERISTICS

STATIC CHARACTERISTICS [1]

PARAMETER		V_{DD} (Vdc)	CONDITIONS	T_{LOW} [2]		+25°C			T_{HIGH} [2]		Units
				Min.	Max.	Min.	Typ.	Max.	Min.	Max.	
QUIESCENT DEVICE CURRENT	I_{DD}	5	$V_{IN}=V_{SS}$ or V_{DD}	–	5	–	0.05	5	–	150	µAdc
		10	All valid input	–	10	–	0.1	10	–	300	
		15	combinations	–	20	–	0.2	20	–	600	
OUTPUT HIGH (SOURCE) CURRENT	I_{OH}										
Decoded outputs		5	V_{OH}=4.6V	-0.175	–	-0.14	-0.28	–	-0.10	–	mAdc
		10	V_{OH}=9.5V	-0.375	–	-0.3	-0.6	–	-0.21	–	
		15	V_{OH}=13.5V	-1.25	–	-1.0	-2.5	–	-0.7	–	
			$V_{IN}=V_{SS}$ or V_{DD}								
Carry output		5	V_{OH}=4.6V	-0.19	–	-0.15	-0.4	–	-0.11	–	mAdc
		10	V_{OH}=9.5V	-0.43	–	-0.35	-1.0	–	-0.25	–	
		15	V_{OH}=13.5V	-1.57	–	-1.25	-4.0	–	-0.88	–	
			$V_{IN}=V_{SS}$ or V_{DD}								
Remaining Outputs		5	V_{OH}=4.6V	-0.10	–	-0.08	-0.2	–	-0.056	–	mAdc
		10	V_{OH}=9.5V	-0.25	–	-0.20	-0.5	–	-0.14	–	
		15	V_{OH}=13.5V	-0.75	–	-0.60	-1.5	–	-0.42	–	
			$V_{IN}=V_{SS}$ or V_{DD}								
OUTPUT LOW (SINK) CURRENT	I_{OL}										
All Outputs Except Carry		5	V_{OL}=0.4V	0.125	–	0.1	0.3	–	0.07	–	mAdc
		10	V_{OL}=0.5V	0.31	–	0.25	0.6	–	0.175	–	
		15	V_{OL}=1.5V	1.44	–	1.15	2.5	–	0.81	–	
			$V_{IN}=V_{SS}$ or V_{DD}								
Carry output		5	V_{OL}=0.4V	0.19	–	0.15	0.4	–	0.11	–	mAdc
		10	V_{OL}=0.5V	0.45	–	0.35	1.0	–	0.25	–	
		15	V_{OL}=1.5V	1.57	–	1.25	4.0	–	0.88	–	
			$V_{IN}=V_{SS}$ or V_{DD}								

NOTES: [1] Remaining Static Electrical Characteristics are listed under "4000B Series Family Specifications".
[2] T_{LOW} = -55°C for C

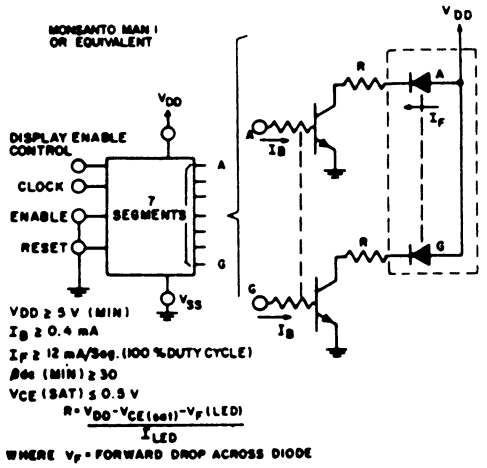
T_{HIGH} = +125°C for C

DYNAMIC CHARACTERISTICS (C_L = 50pF, T_A = 25°C)

PARAMETER		V_{DD} (Vdc)	Min.	Typ.	Max.	Units
CLOCKED OPERATION						
PROPAGATION DELAY TIME Clock to Decoded Outputs	t_{PLH}, t_{PHL}	5	–	500	1000	ns
		10	–	225	450	
		15	–	175	350	
Clock to Carry Out	t_{PLH}, t_{PHL}	5	–	450	900	ns
		10	–	125	250	
		15	–	100	200	
OUTPUT TRANSITION TIME Decoded Outputs	t_{TLH}, t_{THL}	5	–	250	500	ns
		10	–	125	250	
		15	–	100	200	
Carry Output	t_{TLH}, t_{THL}	5	–	200	400	ns
		10	–	100	200	
		15	–	80	160	
MINIMUM CLOCK OR ENABLE PULSE WIDTH	PW_{CL}, PW_{CE}	5	–	200	400	ns
		10	–	100	200	
		15	–	80	160	
MAXIMUM CLOCK FREQUENCY	f_{CL}	5	1.25	2.5	–	MHz
		10	2.5	5.0	–	
		15	3.0	6.0	–	
MAXIMUM CLOCK OR ENABLE RISE AND FALL TIME	t_{rCL}, t_{fCL}	5	15	–	–	µs
		10	15	–	–	
		15	3	–	–	
MINIMUM CLOCK OR ENABLE SETUP TIME	t_{setup}	5	–	250	500	ns
		10	–	100	200	
		15	–	80	160	
RESET OPERATION						
PROPAGATION DELAY TIME Reset to Decoded Outputs	t_{PLH}, t_{PHL}	5	–	700	1400	ns
		10	–	250	500	
		15	–	200	400	
Reset to Carry Output	t_{PLH}, t_{PHL}	5	–	500	1000	ns
		10	–	125	250	
		15	–	100	200	
MINIMUM RESET PULSE WIDTH	PW_R	5	–	200	400	ns
		10	–	100	200	
		15	–	80	160	
RESET REMOVAL TIME	t_{rem}	5	–	375	750	ns
		10	–	150	300	
		15	–	125	250	

DISPLAY INTERFACE

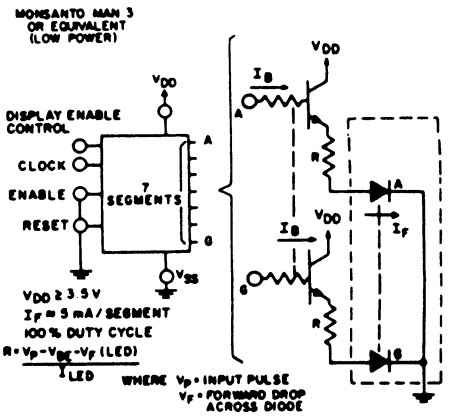
LIGHT EMITTING DIODE DISPLAYS



$V_{DD} \geq 5$ V (MIN)
$I_B \geq 0.4$ mA
$I_F \geq 12$ mA/Seg. (100 % DUTY CYCLE)
β_{dc} (MIN) ≥ 30
V_{CE} (SAT) ≤ 0.5 V

$$R = \frac{V_{DD} - V_{CE(sat)} - V_F(LED)}{I_{LED}}$$

WHERE V_F = FORWARD DROP ACROSS DIODE

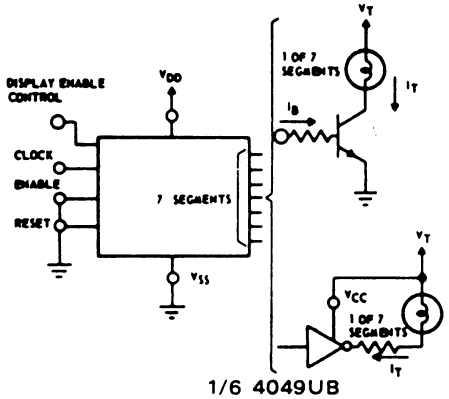


$V_{DD} \geq 3.5$ V
$I_F \approx 5$ mA / SEGMENT
100 % DUTY CYCLE

$$R = \frac{V_P - V_{BE} - V_F(LED)}{I_{LED}}$$

WHERE V_P = INPUT PULSE
V_F = FORWARD DROP ACROSS DIODE

LOW-POWER INCANDESCENT READOUTS



1/6 4049UB

ASSUMED TRANSISTOR CHARACTERISTICS
β_{dc} (min.) $\geq$ 30
$V_{CE(sat.)} \leq$ 0.50 V

@ $V_{DD} \geq$ 3.5 V (min.)
$I_B \geq$ 0.25 mA (min.)
$I_T \leq$ 7.5 mA (min.)

4049UB

@ V_{DD} = 10 V (min.)
V_o "O" $\leq$ 0.6 V
I_T = 8 mA (min.)

@ V_{DD} = 6 V (min.)
V_o "O" $\leq$ 1.0 V
I_T = 5 mA (min.)

$V_T \approx$ 1.5 V TO 3.5 V

INCANDESCENT READOUTS

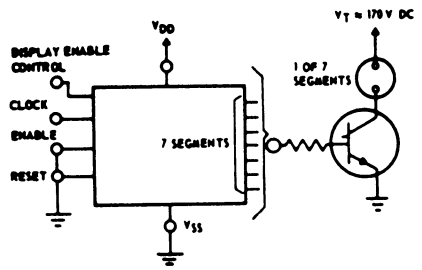
ASSUMED TRANSISTOR CHARACTERISTICS
β_{dc} (min.) $\geq$ 25
$V_{CE(sat.)} \leq$ 0.50 V

@ V_{DD} = 8 V (min.)
I_B = 1.0 mA (min.)
I_T = 24 mA (min.)

4049UB

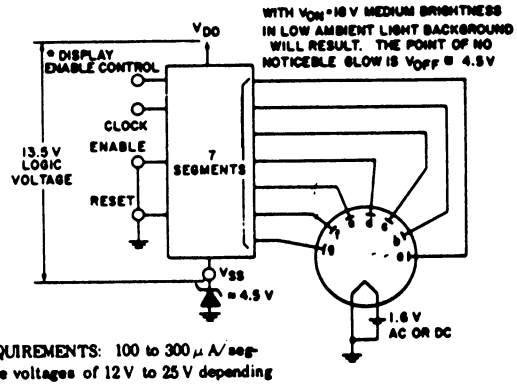
@ V_{DD} = 10 V (min.)
V_o "O" $\leq$ 2 V
I_T = 20 mA (min.)
$V_T \approx$ 3.5 V TO 6 V

NEON READOUTS



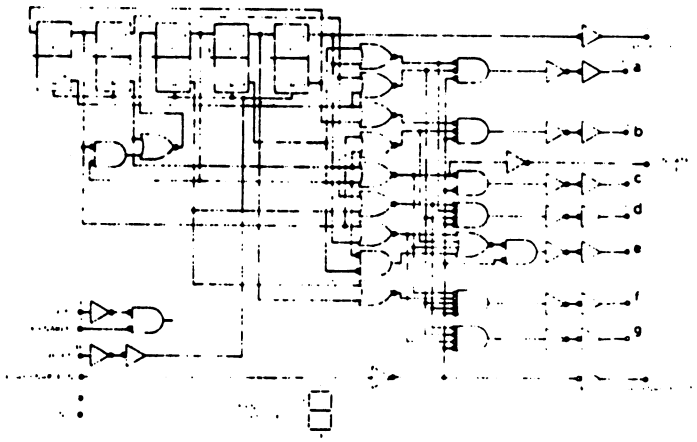
TRANSISTOR CHARACTERISTICS
Leakage with transistor cutoff $\leq$ 0.05 mA
$V_{(BR)CER}$ ··· $> V_T$
β_{dc}(min) $\geq$ 30

LOW-VOLTAGE VACUUM FLUORESCENT READOUTS

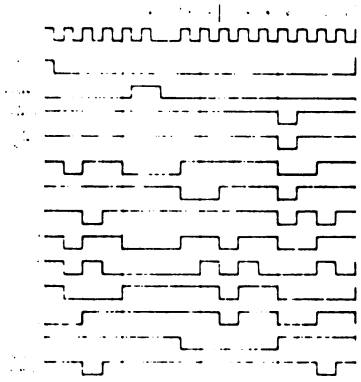


TUBE REQUIREMENTS: 100 to 300 μA/segment at tube voltages of 12 V to 25 V depending on required brightness. Filament requirement 45 mA at 1.6 V, AC or DC.

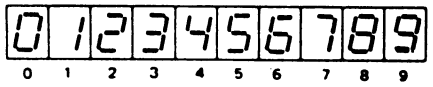
LOGIC DIAGRAM



TIMING DIAGRAM

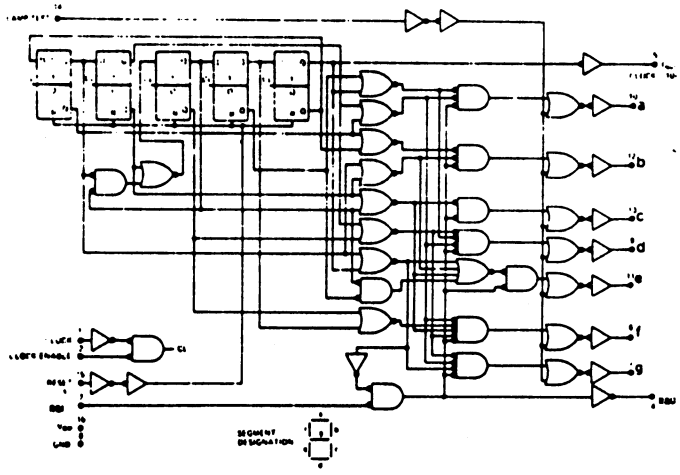


DISPLAY

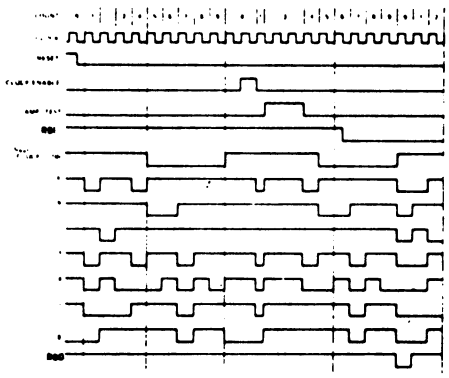


4026AB Decade Counter/7-Segment Decoder with Display Enable

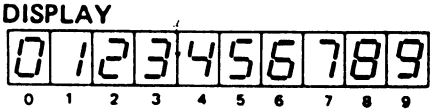
LOGIC DIAGRAM



TIMING DIAGRAM



DISPLAY



4033AB Decade Counter/7-Segment Decoder with Ripple Blanking