

SN54290, SN54293, SN54LS290, SN54LS293 SN74290, SN74293, SN74LS290, SN74LS293 DECADE AND 4-BIT BINARY COUNTERS

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'290, 'LS290 . . . DECADE COUNTERS
'293, 'LS293 . . . 4-BIT BINARY COUNTERS

SN54290, SN54LS290, SN54293,
SN54LS293 . . . J OR W PACKAGE
SN74290, SN74293 . . . N PACKAGE
SN74LS290, SN74LS293 . . . D OR N PACKAGE
(TOP VIEW)

- GND and V_{CC} on Corner Pins
(Pins 7 and 14 Respectively)

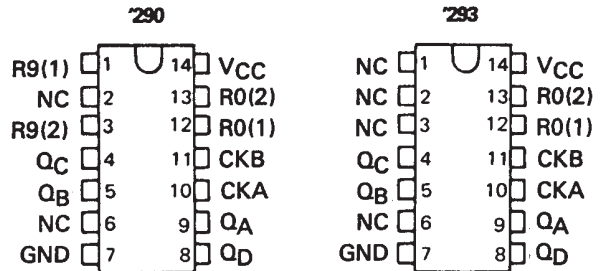
description

The SN54290/SN74290, SN54LS290/SN74LS290, SN54293/SN74293, and SN54LS293/SN74LS293 counters are electrically and functionally identical to the SN5490A/SN7490A, SN54LS90/SN74LS90, SN5493A/SN7493A, and SN54LS93/SN74LS93, respectively. Only the arrangement of the terminals has been changed for the '290, 'LS290, '293, and 'LS293.

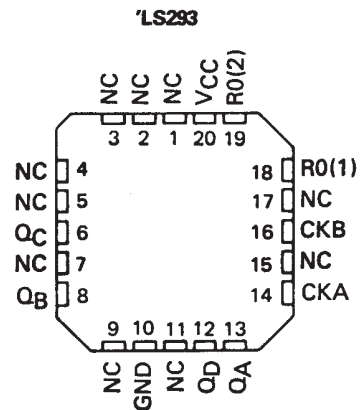
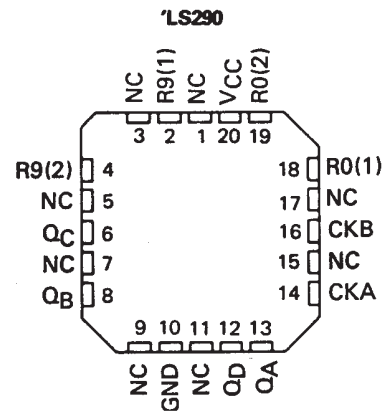
Each of these monolithic counters contains four master-slave flip-flops and additional gating to provide a divide-by-two counter and a three-stage binary counter for which the count cycle length is divide-by-five for the '290 and 'LS290 and divide-by-eight for the '293 and 'LS293.

All of these counters have a gated zero reset and the '290 and 'LS290 also have gated set-to-nine inputs for use in BCD nine's complement applications.

To use the maximum count length (decade or four-bit binary) of these counters, the B input is connected to the Q_A output. The input count pulses are applied to input A and the outputs are as described in the appropriate function table. A symmetrical divide-by-ten count can be obtained from the '290 and 'LS290 counters by connecting the Q_D output to the A input and applying the input count to the B input which gives a divide-by-ten square wave at output Q_A.



SN54LS290, SN54LS293 . . . FK PACKAGE
(TOP VIEW)

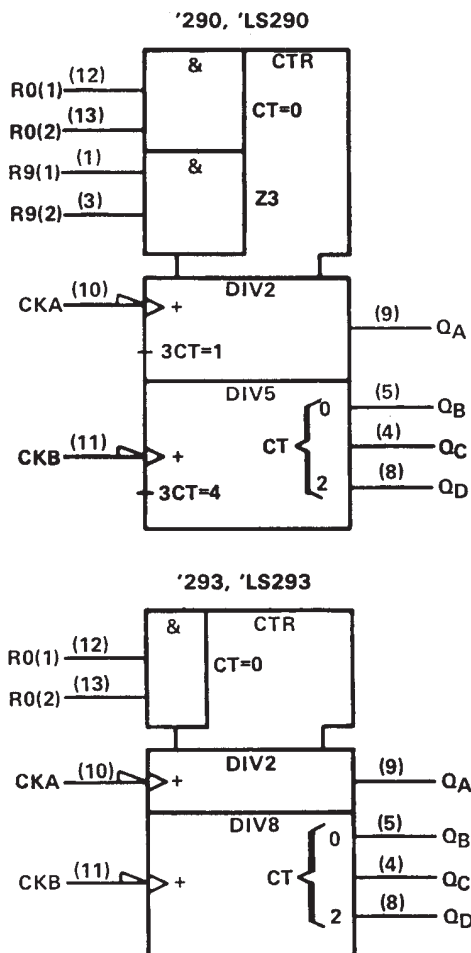


NC - No internal connection

SN54290, SN54293, SN54LS290, SN54LS293
 SN74290, SN74293, SN74LS290, SN74LS293
 DECADE AND 4-BIT BINARY COUNTERS

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logic symbols†

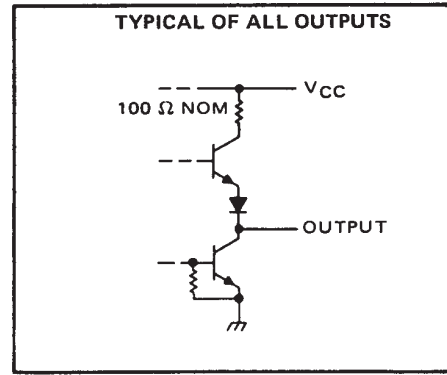
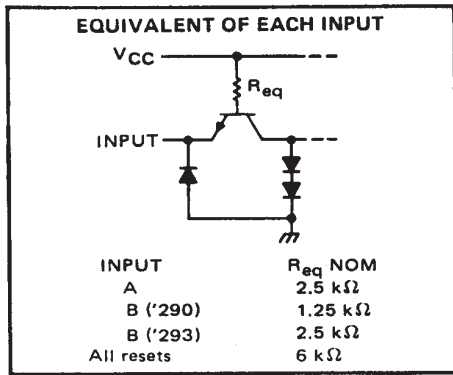


† These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12. Pin numbers shown are for D, J, N, and W packages.

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schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage	5.5 V
Interemitter voltage (see Note 2)	5.5 V
Operating free-air temperature range: SN54' Circuits	-55°C to 125°C
SN74' Circuits	0°C to 70°C
Storage temperature range	-65°C to 150°C

- NOTES: 1. Voltage values, except interemitter voltage, are with respect to network ground terminal.
2. This is the voltage between two emitters of a multiple-emitter transistor. For these circuits, this rating applies between the two R_0 inputs, and for the '290 circuit, it also applies between the two R_9 inputs.

recommended operating conditions

	SN54'			SN74'			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			-800			-800	μ A
Low-level output current, I_{OL}			16			16	mA
Count frequency, f_{count}	A input	0	32	0	32		MHz
	B input	0	16	0	16		
Pulse width, t_w	A input	15		15			ns
	B input	30		30			
	Reset inputs	15		15			
Reset inactive-state setup time, t_{su}	25			25			ns
Operating free-air temperature, T_A	-55		125	0		70	°C

SN54290, SN54293, SN54LS290, SN54LS293
 SN74290, SN74293, SN74LS290, SN74LS293
 DECADE AND 4-BIT BINARY COUNTERS

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	'290			'293			UNIT	
		MIN	TYP‡	MAX	MIN	TYP‡	MAX		
V _{IH} High-level input voltage		2			2			V	
V _{IL} Low-level input voltage				0.8			0.8	V	
V _{IK} Input clamp voltage	V _{CC} = MIN, I _I = -12 mA			-1.5			-1.5	V	
V _{OH} High-level output voltage	V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = 0.8 V, I _{OH} = -800 μA	2.4	3.4		2.4	3.4		V	
V _{OL} Low-level output voltage	V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = 0.8 V, I _{OL} = 16 mA¶		0.2	0.4		0.2	0.4	V	
I _I Input current at maximum input voltage	V _{CC} = MAX, V _I = 5.5 V			1			1	mA	
I _{IH} High-level input current	Any reset			40			40	μA	
	A input	V _{CC} = MAX, V _I = 2.4 V							80
	B input								120
I _{IL} Low-level input current	Any reset	V _{CC} = MAX, V _I = 0.4 V						-1.6	
	A input							-3.2	-3.2
	B input							-4.8	-3.2
I _{OS} Short-circuit output current§	V _{CC} = MAX	SN54'	-20	-57	-20	-57	mA		
		SN74'	-18	-57	-18	-57			
I _{CC} Supply current	V _{CC} = MAX, See Note 3		29	42		26	39	mA	

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.

§ Not more than one output should be shorted at a time.

¶ Q_A outputs are tested at I_{OL} = 16 mA plus the limit value of I_{IL} for the B input. This permits driving the B input while maintaining full fan-out capability.

NOTE 3: I_{CC} is measured with all outputs open, both R₀ inputs grounded following momentary connection to 4.5 V, and all other inputs grounded.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER#	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	'290			'293			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
f _{max}	A	Q _A	C _L = 15 pF, R _L = 400 Ω, See Note 4	32	42		32	42	MHz	
	B	Q _B		16			16			
t _{PLH}	A	Q _A		10	16		10	16	ns	
t _{PHL}				12	18		12	18		
t _{PLH}	A	Q _D		32	48		46	70	ns	
t _{PHL}				34	50		46	70		
t _{PLH}	B	Q _B		10	16		10	16	ns	
t _{PHL}				14	21		14	21		
t _{PLH}	B	Q _C		21	32		21	32	ns	
t _{PHL}				23	35		23	35		
t _{PLH}	B	Q _D		21	32		34	51	ns	
t _{PHL}				23	35		34	51		
t _{PHL}	Set-to-0	Any		26	40		26	40	ns	
t _{PLH}	Set-to-9	Q _A , Q _D		20	30				ns	
t _{PHL}		Q _B , Q _C		26	40					

f_{max} = maximum count frequency

t_{PLH} = propagation delay time, low-to-high-level output

t_{PHL} = propagation delay time, high-to-low-level output

NOTE 4: Load circuits and voltage waveforms are shown in Section 1.



SN54290, SN54293, SN54LS290, SN54LS293
 SN74290, SN74293, SN74LS290, SN74LS293
 DECADE AND 4-BIT BINARY COUNTERS

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†	SN54LS'			SN74LS'			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V _{IH}	High-level input voltage		2			2			V
V _{IL}	Low-level input voltage				0.7			0.8	V
V _{IK}	Input clamp voltage	V _{CC} = MIN, I _I = -18 mA			-1.5			-1.5	V
V _{OH}	High-level output voltage	V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = V _{IL} max, I _{OH} = -400 µA	2.5	3.4		2.7	3.4		V
V _{OL}	Low-level output voltage	V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = V _{IL} max	I _{OL} = 4 mA¶		0.25	0.4	0.25 0.4		V
			I _{OL} = 8 mA¶				0.35	0.5	
I _I	Input current at maximum input voltage	Any reset	V _{CC} = MAX, V _I = 7 V			0.1 0.1			mA
		A input				0.2 0.2			
		B of 'LS290	V _{CC} = MAX, V _I = 5.5 V			0.4 0.4			
		B of 'LS293				0.2 0.2			
I _{IH}	High-level input current	Any reset	V _{CC} = MAX, V _I = 2.7 V			20 20			µA
		A input				40 40			
		B of 'LS290				80 80			
		B of 'LS293				40 40			
I _{IL}	Low-level input current	Any reset	V _{CC} = MAX, V _I = 0.4 V			-0.4 -0.4			mA
		A input				-2.4 -2.4			
		B of 'LS290				-3.2 -3.2			
		B of 'LS293				-1.6 -1.6			
I _{OS}	Short-circuit output current§	V _{CC} = MAX	-20	-100	-20	-100			mA
I _{CC}	Supply current	V _{CC} = MAX, See Note 3	'LS290		9	15	9 15		mA
			'LS293		9	15	9 15		

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.

§ Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

¶ Q_A outputs are tested at specified I_{OL} plus the limit value of I_{IL} for the B input. This permits driving the B input while maintaining full fan-out capability.

NOTE 3: I_{CC} is measured with all outputs open, both R₀ inputs grounded following momentary connection to 4.5 V, and all other inputs grounded.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER#	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	'LS290			'LS293			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
f _{max}	A	Q _A	C _L = 15 pF, R _L = 2 kΩ, See Note 4	32	42		32	42		MHz
	B	Q _B		16			16			
t _{PLH}	A	Q _A		10	16		10	16		ns
t _{PHL}				12	18		12	18		
t _{PLH}	A	Q _D		32	48		46	70		ns
t _{PHL}				34	50		46	70		
t _{PLH}	B	Q _B		10	16		10	16		ns
t _{PHL}				14	21		14	21		
t _{PLH}	B	Q _C		21	32		21	32		ns
t _{PHL}				23	35		23	35		
t _{PLH}	B	Q _D		21	32		34	51		ns
t _{PHL}				23	35		34	51		
t _{PHL}	Set-to-0	Any		26	40		26	40		ns
t _{PLH}	Set-to-9	Q _A , Q _D		20	30					ns
t _{PHL}		Q _B , Q _C	26	40						

#f_{max} = maximum count frequency

t_{PLH} = propagation delay time, low-to-high-level output

t_{PHL} = propagation delay time, high-to-low-level output

NOTE 4: Load circuits and voltage waveforms are shown in Section 1.



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