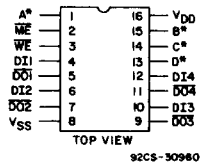
CD40114B **Preliminary Data**

COS/MOS 64-Bit Random Access Memory

High-Voltage Types (20-Volt Rating)

Features:

- **Input address latch**
- **3-state outputs**
- **Low-power TTL compatible**
- **Equivalent to and pin-compatible with National 74C89**
- **Pin -compatible with 74S189**
- **Buffered inputs and outputs**
- **100% tested for quiescent current at 20 V**
- **Standardized, symmetrical output characteristics**
- **5-V, 10-V, and 15-V parametric ratings**
- **Meets all requirements of JEDEC Tentative Standard No. 13A, "Standard Specifications for description of "B" Series CMOS Devices"**



Terminal Assignment

The RCA-CD40114B is a 16-word x 4-bit random access memory (RAM) with four address inputs, four data inputs, a WRITE ENABLE ($\overline{WE}$) input, a MEMORY ENABLE ($\overline{ME}$) input, and four 3-state data outputs. The four address inputs are decoded internally to select one of the 16 possible word locations. The address information is latched on the negative edge of the $\overline{ME}$ input by an internal address register. The selected output assumes a high-impedance condition when the device is writing or disabled. The $\overline{ME}$ input and the 3-state outputs allow memory expansion.

Applications:

- **Main frame memories**
- **Memory storage**
- **Scratch-pad memories**
- **Games**

$\overline{ME}$	$\overline{WE}$	OPERATION	CONDITION OF OUTPUTS
L	L	Write	3-STATE
L	H	Read	Complement of Selected Word
H	L	Inhibit, Storage	3-STATE
H	H	Inhibit, Storage	3-STATE

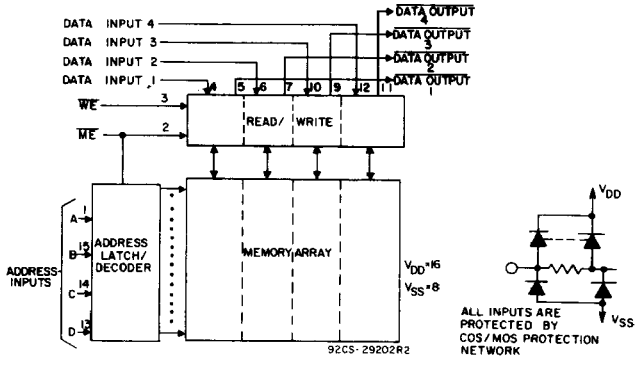


Fig. 1 — Functional Block Diagram

Address Operation

The high-to-low transition of $\overline{ME}$ enables the memory. Address inputs must be stable (either high or low) prior to and during this transition, but it is not necessary to hold them stable beyond it.

Write Operation

When $\overline{WE}$ and $\overline{ME}$ are low, information present at the data inputs is written into the memory at the selected address.

Read Operation

When $\overline{ME}$ is low and $\overline{WE}$ is high the complement of the memory contents at the selected address location are non-destructively read out at the four data outputs.

The CD40114B is supplied in 16-lead hermetic dual-in-line ceramic packages (D and F suffixes), 16-lead plastic packages (E suffix), and in chip form (H suffix).

RECOMMENDED OPERATING CONDITIONS

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range (For T_A = Full Package Temperature Range)	3	18	V

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{DD})
(Voltages referenced to V_{SS} Terminal) . . . . . −0.5 to +20 V
INPUT VOLTAGE RANGE, ALL INPUTS . . . . . −0.5 to V_{DD} +0.5 V
DC INPUT CURRENT, ANY ONE INPUT . . . . . ±10 mA
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = −40 to +60°C (PACKAGE TYPE E) . . . . . 500 mW
For T_A = +60 to +85°C (PACKAGE TYPE E) . . . . . Derate Linearly at 12 mW/°C to 200 mW
For T_A = −55 to +100°C (PACKAGE TYPES D, F) . . . . . 500 mW
For T_A = +100 to +125°C (PACKAGE TYPES D, F) . . . Derate Linearly at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR
FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (All Package Types) . . . . . 100 mW
OPERATING-TEMPERATURE RANGE (T_A):
PACKAGE TYPES D, F, H . . . . . −55 to +125°C
PACKAGE TYPE E . . . . . −40 to +85°C
STORAGE TEMPERATURE RANGE (T_{stg}) . . . . . −65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max. . . . . +265°C

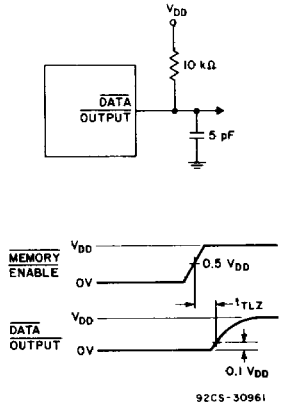


Fig. 2 — Output low to high-impedance transition time test circuit and waveforms.

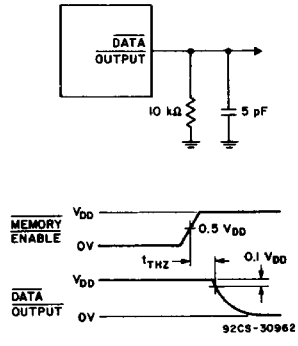


Fig. 3 — Output high to high-impedance transition time test circuit and waveforms.

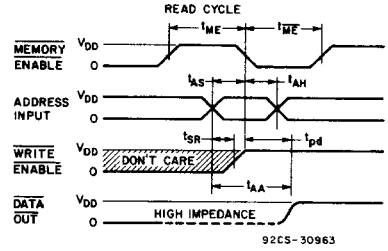


Fig. 4 – Read cycle waveforms.

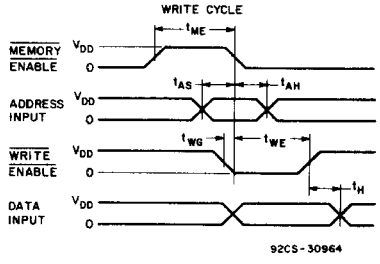


Fig. 5 – Write cycle waveforms

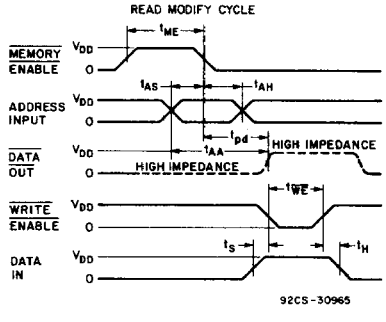


Fig. 6 – Read-modify-write cycle waveforms.

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C) Values at −55, +25, +125 Apply to D, F, H Packages Values at −40, +25, +85 Apply to E Package							UNITS
								+25			
	V_O (V)	V_{IN} (V)	V_{DD} (V)	−55	−40	+85	+125	Min.	Typ.	Max.	
Quiescent Device Current, I_{DD} Max.	–	0,5	5	5	5	150	150	–	0.04	5	μA
	–	0,10	10	10	10	300	300	–	0.04	10	
	–	0,15	15	20	20	600	600	–	0.04	20	
	–	0,20	20	100	100	3000	3000	–	0.08	100	
Output Low (Sink) Current I_{OL} Min.	0.4	0,5	5	0.64	0.61	0.42	0.36	0.51	1	–	mA
	0.5	0,10	10	1.6	1.5	1.1	0.9	1.3	2.6	–	
	1.5	0,15	15	4.2	4	2.8	2.4	3 4	6.8	–	
Output High (Source) Current, I_{OH} Min.	4.6	0,5	5	−0.64	−0.61	−0.42	−0.36	−0.51	−1	–	
	2.5	0,5	5	−2	−1.8	−1.3	−1.15	−1.6	−3.2	–	
	9.5	0,10	10	−1.6	−1.5	−1.1	−0.9	−1.3	−2.6	–	
	13.5	0,15	15	−4.2	−4	−2.8	−2.4	−3.4	−6.8	–	
Output Voltage: Low-Level, V_{OL} Max.	–	0,5	5	0.05				–	0	0.05	V
	–	0,10	10	0.05				–	0	0.05	
	–	0,15	15	0.05				–	0	0.05	
Output Voltage: High-Level, V_{OH} Min.	–	0,5	5	4.95				4.95	5	–	
	–	0,10	10	9.95				9.95	10	–	
	–	0,15	15	14.95				14.95	15	–	
Input Low Voltage, V_{IL} Max.	0.5, 4.5	–	5	1.5				—	—	1.5	V
	1, 9	–	10	3				—	—	3	
	1.5,13.5	–	15	4				–	—	4	
Input High Voltage, V_{IH} Min.	0.5, 4.5	–	5	3.5				3.5	—	—	
	1, 9	–	10	7				7	—	—	
	1.5,13.5	–	15	11				11	—	—	
Input Current I_{IN} Max.	–	0,18	18	±0.1	±0.1	±1	±1	–	$\pm 10^{-5}$	±0.1	μA
3-State Output Leakage Current I_{OUT} Max.	0,18	0,18	18	±0.4	±0.4	±12	±12	–	$\pm 10^{-4}$	±0.4	μA

CD40114B

ELECTRICAL CHARACTERISTICS at T_A = 25°C, C_L = 50 pF, R_L = 200 kΩ, t_r, t_f = 20 ns
Unless Otherwise Specified

CHARACTERISTIC	TEST CONDITIONS	V_{DD} (V)	LIMITS Typ.	LIMITS Max.	UNITS
Access Time From Address Change, t_{AA}		5	325	650	ns
		10	140	280	
		15	120	240	
Min. Address Setup Time, t_{AS}		5	75	150	ns
		10	30	60	
		15	25	50	
Min. Address Hold Time, t_{AH}		5	30	60	ns
		10	20	40	
		15	15	30	
Min. $\overline{\text{Memory Enable}}$ Pulse Width, $t_{\overline{ME}}$, t_{ME}		5	200	400	ns
		10	75	150	
		15	60	120	
Min. $\overline{\text{Write Enable}}$ Setup Time For a Read, t_{SR}		5	–	0	ns
		10	–	0	
		15	–	0	
Min. $\overline{\text{Write Enable}}$ Setup Time for a Write, t_{WS}		5	–	t_{ME}	ns
		10	–	t_{ME}	
		15	–	t_{ME}	
Min. $\overline{\text{Write Enable}}$ Pulse Width, $t_{\overline{WE}}$		5	150	300	ns
		10	50	100	
		15	40	80	
Min. Data Input Hold Time, t_H		5	25	50	ns
		10	12	25	
		15	10	20	
Min. Data Input Setup Time, t_S		5	25	50	ns
		10	12	25	
		15	10	20	
Propagation Delay Time from Output-high or Output-low to High-Impedance State from $\overline{\text{Memory Enable}}$	R_L = 10 kΩ, C_L = 5 pF	5	150	300	ns
		10	60	120	
		15	50	100	
Propagation Delay Time from Output-high or Output-low to High-Impedance State from $\overline{\text{Write Enable}}$	R_L = 10 kΩ, C_L = 5 pF	5	150	300	ns
		10	60	120	
		15	50	100	
Propagation Delay Time From $\overline{\text{Memory Enable}}$, t_{pd}		5	250	500	ns
		10	100	200	
		15	80	160	
Input Capacitance, C_{IN}	Any Input		5	7.5	pF
Output Capacitance, C_{OUT}	Any Output		6.5	13	pF