



**2N7000**  
**2N7002**

**N-CHANNEL 60V - 1.8Ω - 0.35A SOT23-3L - TO-92**  
**STripFET™II POWER MOSFET**

PRELIMINARY DATA

TYPE	V <sub>DSS</sub>	R <sub>DS(on)</sub>	I <sub>D</sub>
2N7000	60 V	< 5 Ω (@ 10V)	0.35 A
2N7002	60 V	< 5 Ω (@ 10V)	0.20 A

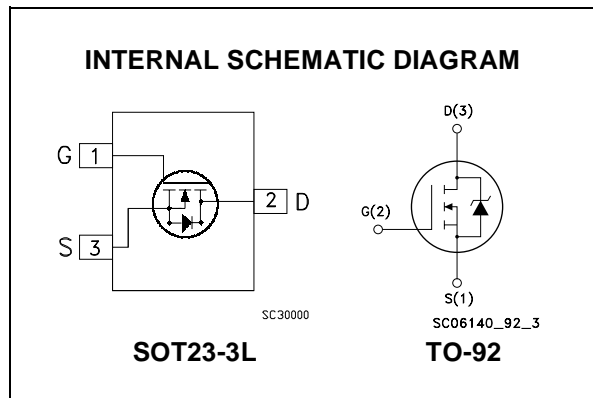
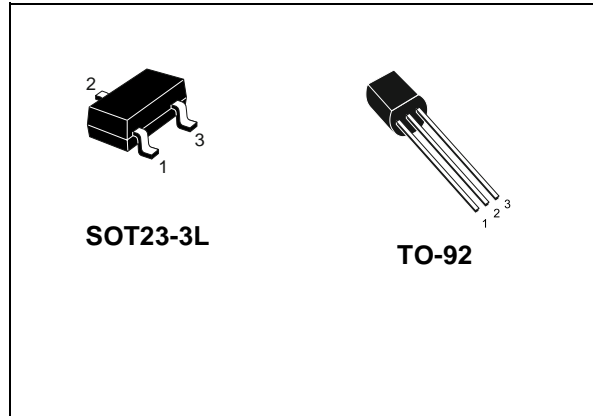
- TYPICAL R<sub>DS(on)</sub> = 1.8Ω @10V
- LOW Q<sub>g</sub>
- LOW THRESHOLD DRIVE

**DESCRIPTION**

This Power MOSFET is the second generation of STMicroelectronics unique "Single Feature Size™" strip-based process. The resulting transistor shows extremely high packing density for low on-resistance, rugged avalanche characteristics and less critical alignment steps therefore a remarkable manufacturing reproducibility.

**APPLICATIONS**

- HIGH SWITCHING APPLICATIONS



**ORDER CODE**

PART NUMBER	MARKING	PACKAGE	PACKAGING
2N7000	2N7000G	TO-92	BULK
2N7002	ST2N	SOT23-3L	TAPE & REEL

## 2N7000 - 2N7002

### ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value		Unit
		TO-92	STO23-3L	
$V_{DS}$	Drain-source Voltage ( $V_{GS} = 0$ )	60		V
$V_{DGR}$	Drain-gate Voltage ( $R_{GS} = 20\text{ k}\Omega$ )	60		V
$V_{GS}$	Gate- source Voltage	$\pm 18$		V
$I_D$	Drain Current (continuous) at $T_C = 25^\circ\text{C}$	0.35	0.25	A
$I_{DM} (\bullet)$	Drain Current (pulsed)	1.4	1	A
$P_{TOT}$	Total Dissipation at $T_C = 25^\circ\text{C}$	1	0.35	W

( $\bullet$ )Pulse width limited by safe operating area

### THERMAL DATA

		TO-92	SOT23-3L	
$R_{thj-amb}$	Thermal Resistance Junction-ambient Max	125	357.1 (*)	$^\circ\text{C}/\text{W}$
$T_J$ $T_{stg}$	Operating Junction Temperature Storage Temperature	- 55 to 150		$^\circ\text{C}$

(\*) DEVICE MOUNTED ON A PCB AREA OF  $1\text{cm}^2$

### ON/OFF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source Breakdown Voltage	$I_D = 250\ \mu\text{A}$ , $V_{GS} = 0$	60			V
$I_{DSS}$	Zero Gate Voltage Drain Current ( $V_{GS} = 0$ )	$V_{DS} = \text{Max Rating}$ $V_{DS} = \text{Max Rating}$ , $T_C = 125^\circ\text{C}$			1 10	$\mu\text{A}$ $\mu\text{A}$
$I_{GSS}$	Gate-body Leakage Current ( $V_{DS} = 0$ )	$V_{GS} = \pm 18\text{ V}$			$\pm 100$	nA
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}$ , $I_D = 250\ \mu\text{A}$	1			V
$R_{DS(on)}$	Static Drain-source On Resistance	$V_{GS} = 10\text{ V}$ , $I_D = 0.5\text{ A}$ $V_{GS} = 4.5\text{ V}$ , $I_D = 0.5\text{ A}$		1.8 2	5 5.3	$\Omega$ $\Omega$

**ELECTRICAL CHARACTERISTICS** ( $T_{CASE} = 25\text{ }^{\circ}\text{C}$  UNLESS OTHERWISE SPECIFIED)  
**DYNAMIC**

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$g_{fs}$ (1)	Forward Transconductance	$V_{DS} = 10\text{ V}$ , $I_D = 0.5\text{ A}$		0.6		S
$C_{iss}$ $C_{oss}$ $C_{rss}$	Input Capacitance Output Capacitance Reverse Transfer Capacitance	$V_{DS} = 25\text{ V}$ , $f = 1\text{ MHz}$ , $V_{GS} = 0$		43 20 6		pF pF pF

**SWITCHING ON**

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$ $t_r$	Turn-on Delay Time Rise Time	$V_{DD} = 30\text{ V}$ , $I_D = 0.5\text{ A}$ $R_G = 4.7\Omega$ , $V_{GS} = 4.5\text{ V}$ (see test circuit, Figure 1)		5 15		ns ns
$Q_g$ $Q_{gs}$ $Q_{gd}$	Total Gate Charge Gate-Source Charge Gate-Drain Charge	$V_{DD} = 30\text{ V}$ , $I_D = 1\text{ A}$ , $V_{GS} = 5\text{ V}$ (see test circuit, Figure 2)		1.4 0.8 0.5	2	nC nC nC

**SWITCHING OFF**

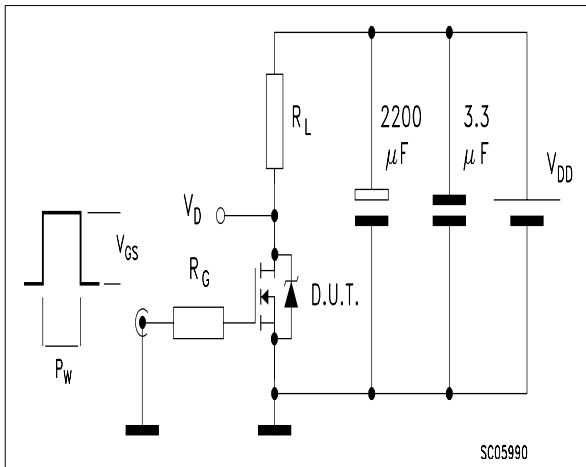
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(off)}$ $t_f$	Turn-Off Delay Time Fall Time	$V_{DD} = 30\text{ V}$ , $I_D = 0.5\text{ A}$ , $R_G = 4.7\Omega$ , $V_{GS} = 4.5\text{ V}$ (see test circuit, Figure 1)		7 8		ns ns

**SOURCE DRAIN DIODE**

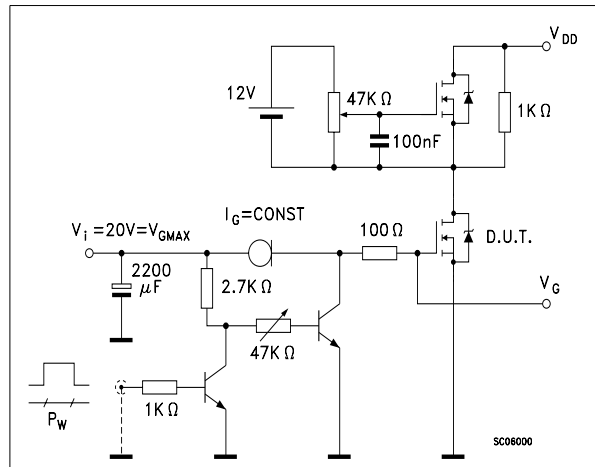
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$I_{SD}$ $I_{SDM}$ (2)	Source-drain Current Source-drain Current (pulsed)				0.35 1.40	A A
$V_{SD}$ (1)	Forward On Voltage	$I_{SD} = 1\text{ A}$ , $V_{GS} = 0$			1.2	V
$t_{rr}$ $Q_{rr}$ $I_{RRM}$	Reverse Recovery Time Reverse Recovery Charge Reverse Recovery Current	$I_{SD} = 1\text{ A}$ , $di/dt = 100\text{ A}/\mu\text{s}$ , $V_{DD} = 20\text{ V}$ , $T_j = 150^{\circ}\text{C}$ (see test circuit, Figure 3)		32 25 1.6		ns nC A

Note: 1. Pulsed: Pulse duration = 300  $\mu\text{s}$ , duty cycle 1.5 %.  
2. Pulse width limited by safe operating area.

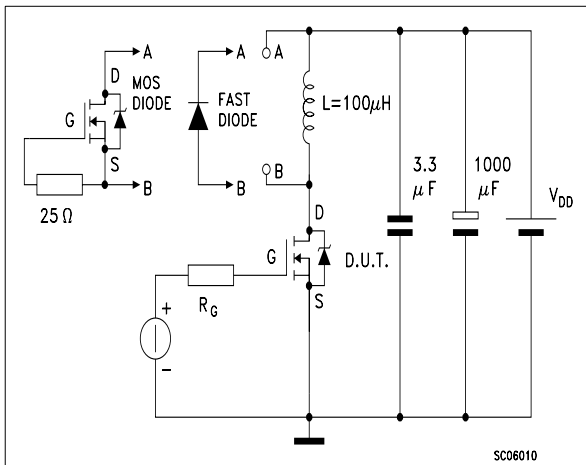
**Fig. 1: Switching Times Test Circuit For Resistive Load**



**Fig. 2: Gate Charge test Circuit**

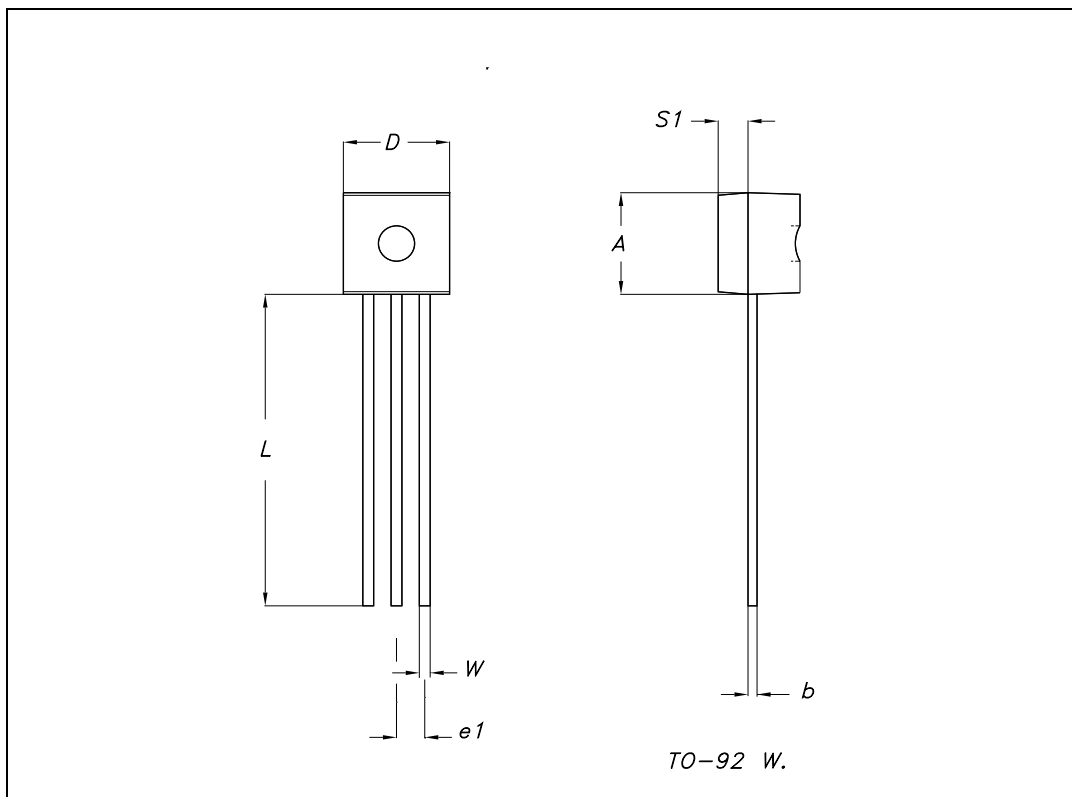


**Fig. 3: Test Circuit For Diode Recovery Behaviour**



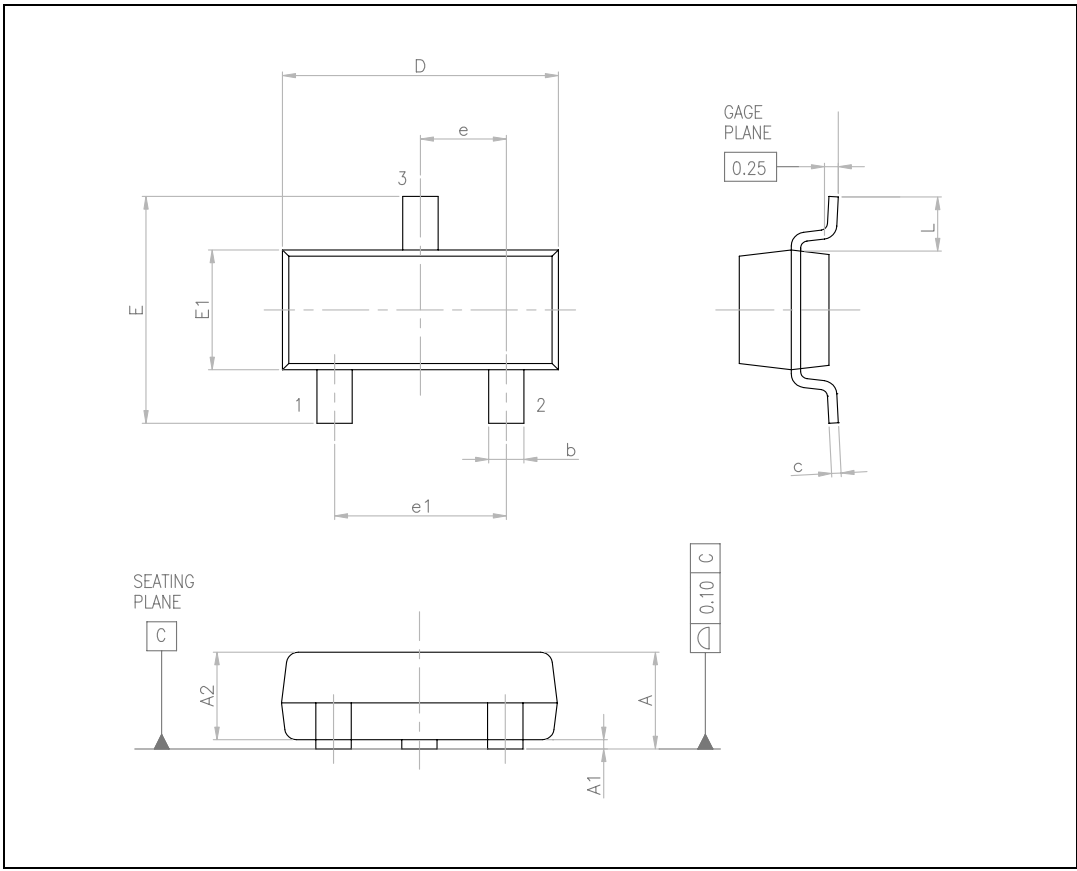
<b>TO-92 MECHANICAL DATA</b>
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DIM.	mm.			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	4.38		4.78	0.17		0.188
b	0.33		0.48	0.013		0.018
D	4.43		4.83	0.174		0.190
E			3.86			0.152
e1	1.07		1.74	0.042		0.068
L	14.07		14.87	0.553		0.585
S1	0.92		1.12	0.036		0.044
W	0.36		0.56	0.014		0.022
V		4°			4°	



**SOT23-3L MECHANICAL DATA**

DIM.	mm.			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	0.903		1.220	0.035		0.048
A1	0.013		0.100	0.0005		0.004
A2	0.890		1.120	0.035		0.044
b	0.370		0.510	0.014		0.020
C	0.085		0.180	0.003		0.007
D	2.800		3.040	0.110		0.120
E	2.100		2.64	0.082		0.104
E1	1.200		1.400	0.047		0.055
e	0.890		1.030	0.035		0.040
e1	1.780		2.050	0.070		0.080
L	0.400		0.600	0.015		0.023



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