

MC14001UB, MC14011UB

UB-Suffix Series CMOS Gates

The UB Series logic gates are constructed with P and N channel enhancement mode devices in a single monolithic structure (Complementary MOS). Their primary use is where low power dissipation and/or high noise immunity is desired. The UB set of CMOS gates are inverting non-buffered functions.

- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Linear and Oscillator Applications
- Capable of Driving Two Low-power TTL Loads or One Low-power Schottky TTL Load Over the Rated Temperature Range
- Double Diode Protection on All Inputs
- Pin-for-Pin Replacements for Corresponding CD4000 Series UB Suffix Devices

MAXIMUM RATINGS (Voltages Referenced to V_{SS}) (Note 1.)

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage Range	-0.5 to +18.0	V
V_{in}, V_{out}	Input or Output Voltage Range (DC or Transient)	-0.5 to $V_{DD} + 0.5$	V
I_{in}, I_{out}	Input or Output Current (DC or Transient) per Pin	± 10	mA
P_D	Power Dissipation, per Package (Note 2.)	500	mW
T_A	Ambient Temperature Range	-55 to +125	$^{\circ}\text{C}$
T_{stg}	Storage Temperature Range	-65 to +150	$^{\circ}\text{C}$
T_L	Lead Temperature (8-Second Soldering)	260	$^{\circ}\text{C}$

1. Maximum Ratings are those values beyond which damage to the device may occur.
2. Temperature Derating:
Plastic "P and D/DW" Packages: - 7.0 mW/ $^{\circ}\text{C}$ From 65 $^{\circ}\text{C}$ To 125 $^{\circ}\text{C}$

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \leq (V_{in} \text{ or } V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

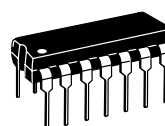


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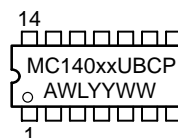
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MC14001UB Quad 2-Input NOR Gate MC14011UB Quad 2-Input NAND Gate

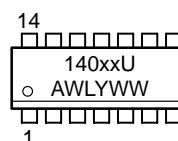
MARKING DIAGRAMS



PDIP-14
P SUFFIX
CASE 646



SOIC-14
D SUFFIX
CASE 751A



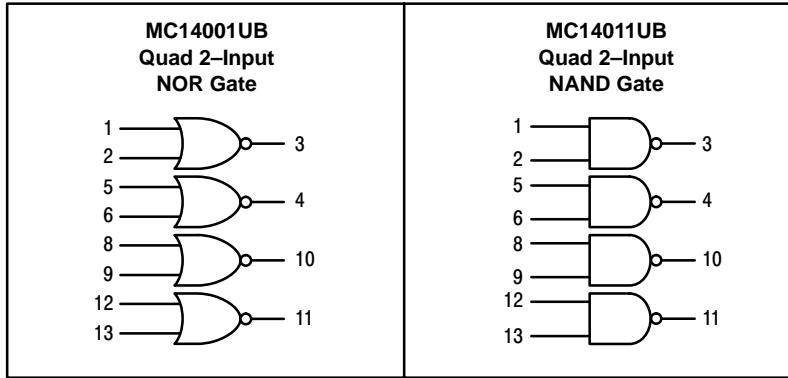
xx = Specific Device Code
A = Assembly Location
WL, L = Wafer Lot
YY, Y = Year
WW, W = Work Week

ORDERING INFORMATION

Device	Package	Shipping
MC14001UBCP	PDIP-14	2000/Box
MC14001UBD	SOIC-14	55/Rail
MC14001UBDR2	SOIC-14	2500/Tape & Reel
MC14011UBCP	PDIP-14	2000/Box
MC14011UBD	SOIC-14	55/Rail
MC14011UBDR2	SOIC-14	2500/Tape & Reel

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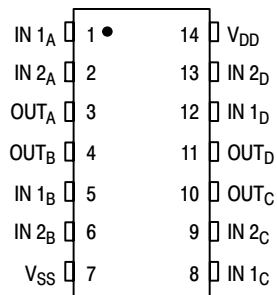
LOGIC DIAGRAMS



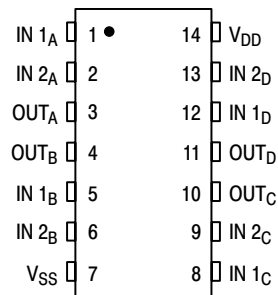
V_{DD} = PIN 14
 V_{SS} = PIN 7
 FOR ALL DEVICES

PIN ASSIGNMENTS

MC14001UB
Quad 2-Input NOR Gate



MC14011UB
Quad 2-Input NAND Gate



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ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Characteristic	Symbol	V_{DD} Vdc	-55°C		25°C			125°C		Unit
			Min	Max	Min	Typ (3.)	Max	Min	Max	
Output Voltage $V_{in} = V_{DD}$ or 0 $V_{in} = 0$ or V_{DD}	"0" Level V_{OL}	5.0	—	0.05	—	0	0.05	—	0.05	Vdc
		10	—	0.05	—	0	0.05	—	0.05	
		15	—	0.05	—	0	0.05	—	0.05	
	"1" Level V_{OH}	5.0	4.95	—	4.95	5.0	—	4.95	—	Vdc
		10	9.95	—	9.95	10	—	9.95	—	
		15	14.95	—	14.95	15	—	14.95	—	
Input Voltage ($V_O = 4.5$ Vdc) ($V_O = 9.0$ Vdc) ($V_O = 13.5$ Vdc) ($V_O = 0.5$ Vdc) ($V_O = 1.0$ Vdc) ($V_O = 1.5$ Vdc)	"0" Level V_{IL}	5.0	—	1.0	—	2.25	1.0	—	1.0	Vdc
		10	—	2.0	—	4.50	2.0	—	2.0	
		15	—	2.5	—	6.75	2.5	—	2.5	
	"1" Level I_{IH}	5.0	4.0	—	4.0	2.75	—	4.0	—	Vdc
		10	8.0	—	8.0	5.50	—	8.0	—	
		15	12.5	—	12.5	8.25	—	12.5	—	
Output Drive Current ($V_{OH} = 2.5$ Vdc) ($V_{OH} = 4.6$ Vdc) ($V_{OH} = 9.5$ Vdc) ($V_{OH} = 13.5$ Vdc) ($V_{OL} = 0.4$ Vdc) ($V_{OL} = 0.5$ Vdc) ($V_{OL} = 1.5$ Vdc)	Source I_{OH}	5.0	-1.2	—	-1.0	-1.7	—	-0.7	—	mAdc
		5.0	-0.25	—	-0.2	-0.36	—	-0.14	—	
		10	-0.62	—	-0.5	-0.9	—	-0.35	—	
		15	-1.8	—	-1.5	-3.5	—	-1.1	—	
	Sink I_{OL}	5.0	0.64	—	0.51	0.88	—	0.36	—	mAdc
		10	1.6	—	1.3	2.25	—	0.9	—	
15		4.2	—	3.4	8.8	—	2.4	—		
Input Current	I_{in}	15	—	± 0.1	—	± 0.00001	± 0.1	—	± 1.0	μ Adc
Input Capacitance ($V_{in} = 0$)	C_{in}	—	—	—	—	5.0	7.5	—	—	pF
Quiescent Current (Per Package)	I_{DD}	5.0	—	0.25	—	0.0005	0.25	—	7.5	μ Adc
		10	—	0.5	—	0.0010	0.5	—	15	
		15	—	1.0	—	0.0015	1.0	—	30	
Total Supply Current (4.) (5.) (Dynamic plus Quiescent, Per Gate $C_L = 50$ pF)	I_T	5.0	$I_T = (0.3 \mu\text{A/kHz}) f + I_{DD}/N$							μ Adc
10	$I_T = (0.6 \mu\text{A/kHz}) f + I_{DD}/N$									
15	$I_T = (0.8 \mu\text{A/kHz}) f + I_{DD}/N$									

3. Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

4. The formulas given are for the typical characteristics only at 25°C.

5. To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50 \text{ pF}) + (C_L - 50) \text{ Vfk}$$

where: I_T is in μH (per package), C_L in pF, $V = (V_{DD} - V_{SS})$ in volts, f in kHz is input frequency, and $k = 0.001 \times$ the number of exercised gates per package.

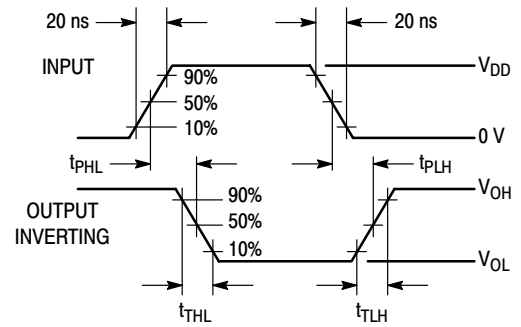
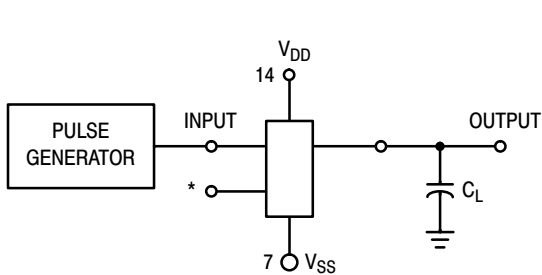
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SWITCHING CHARACTERISTICS (6.) ($C_L = 50 \text{ pF}$, $T_A = 25^\circ\text{C}$)

Characteristic	Symbol	V_{DD} Vdc	Min	Typ (7.)	Max	Unit
Output Rise Time $t_{TLH} = (3.0 \text{ ns/pF}) C_L + 30 \text{ ns}$ $t_{TLH} = (1.5 \text{ ns/pF}) C_L + 15 \text{ ns}$ $t_{TLH} = (1.1 \text{ ns/pF}) C_L + 10 \text{ ns}$	t_{TLH}	5.0 10 15	— — —	180 90 65	360 180 130	ns
Output Fall Time $t_{THL} = (1.5 \text{ ns/pF}) C_L + 25 \text{ ns}$ $t_{THL} = (0.75 \text{ ns/pF}) C_L + 12.5 \text{ ns}$ $t_{THL} = (0.55 \text{ ns/pF}) C_L + 9.5 \text{ ns}$	t_{THL}	5.0 10 15	— — —	100 50 40	200 100 80	ns
Propagation Delay Time $t_{PLH}, t_{PHL} = (1.7 \text{ ns/pF}) C_L + 30 \text{ ns}$ $t_{PLH}, t_{PHL} = (0.66 \text{ ns/pF}) C_L + 22 \text{ ns}$ $t_{PLH}, t_{PHL} = (0.50 \text{ ns/pF}) C_L + 15 \text{ ns}$	t_{PLH}, t_{PHL}	5.0 10 15	— — —	90 50 40	180 100 80	ns

6. The formulas given are for the typical characteristics only at 25°C .

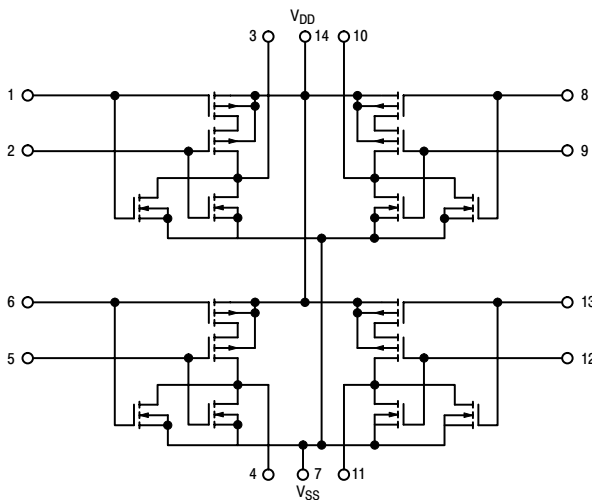
7. Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.



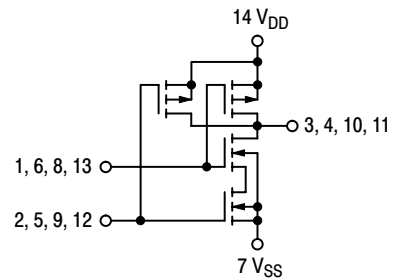
*All unused inputs of AND, NAND gates must be connected to V_{DD} .
 All unused inputs of OR, NOR gates must be connected to V_{SS} .

Figure 1. Switching Time Test Circuit and Waveforms

MC14001UB CIRCUIT SCHEMATIC



MC14011UB CIRCUIT SCHEMATIC (1/4 of Device Shown)



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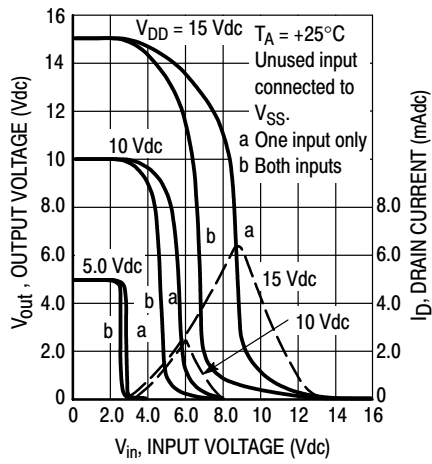


Figure 2. Typical Voltage and Current Transfer Characteristics

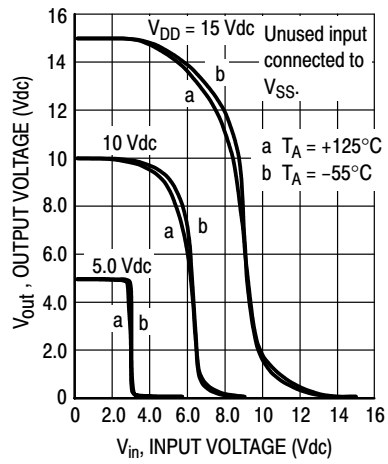


Figure 3. Typical Voltage Transfer Characteristics versus Temperature

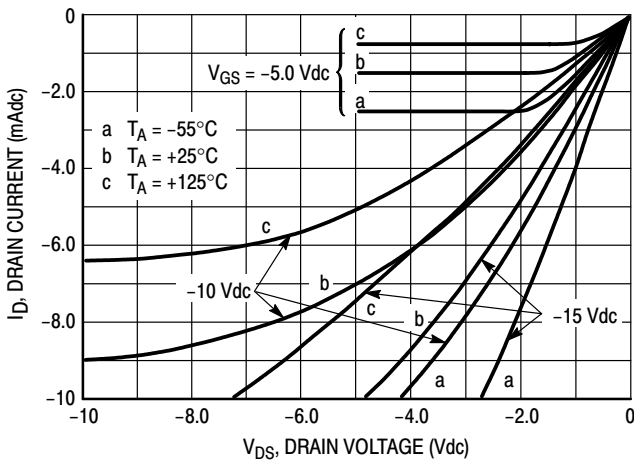


Figure 4. Typical Output Source Characteristics

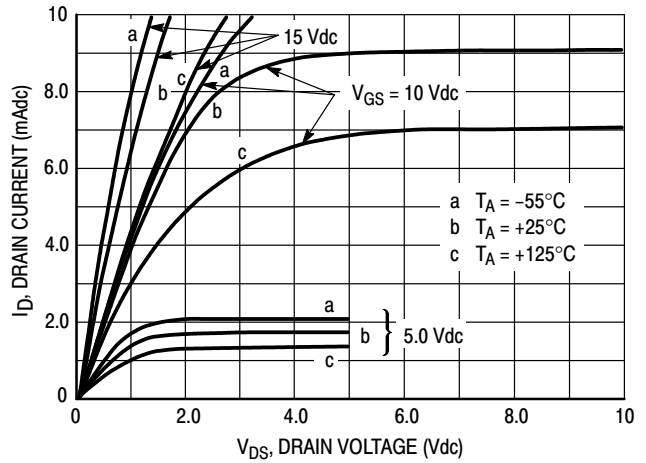
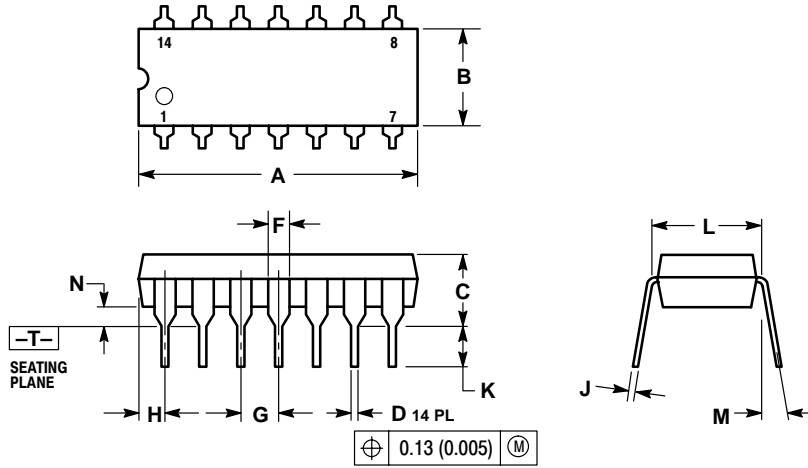


Figure 5. Typical Output Sink Characteristics

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PACKAGE DIMENSIONS

P SUFFIX
PLASTIC DIP PACKAGE
CASE 646-06
ISSUE M



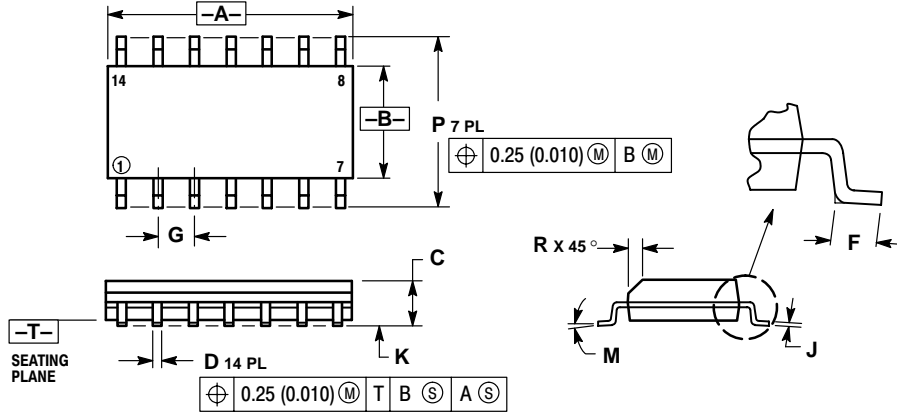
- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: INCH.
 3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
 4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
 5. ROUNDED CORNERS OPTIONAL.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.715	0.770	18.16	18.80
B	0.240	0.260	6.10	6.60
C	0.145	0.185	3.69	4.69
D	0.015	0.021	0.38	0.53
F	0.040	0.070	1.02	1.78
G	0.100 BSC		2.54 BSC	
H	0.052	0.095	1.32	2.41
J	0.008	0.015	0.20	0.38
K	0.115	0.135	2.92	3.43
L	0.290	0.310	7.37	7.87
M	---	10°	---	10°
N	0.015	0.039	0.38	1.01

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PACKAGE DIMENSIONS

D SUFFIX
 PLASTIC SOIC PACKAGE
 CASE 751A-03
 ISSUE F



NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	8.55	8.75	0.337	0.344
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.228	0.244
R	0.25	0.50	0.010	0.019

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